CLAIMS

1. A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; and

automatically generating an output clock signal based on the determination.

2. The method of claim 1 wherein generating the output clock signal comprises generating a single-ended output clock signal when the input clock signal is determined to be a differential clock signal.

3. The method of claim 1 wherein the generated clock signal has the same frequency as the input clock signal.

4. The method of claim 1, wherein receiving the input clock signal comprises receiving a single-ended clock signal on a first input terminal and a ground potential on the second input terminal.

5. The method of claim 1 further comprising generating a clock mode signal based on the determination.

6. A method comprising:

receiving a first input clock signal;

receiving a second input clock signal, wherein the second input clock signal is one of a constant signal at ground potential, a constant signal above ground potential or a signal at the same frequency as the first input clock signal;

automatically generating a single-ended clock signal from the first and second input clock signals when the second input clock signal is one of a constant signal above ground potential or a signal at the same frequency as the first input clock signal; and

automatically generating a single-ended clock signal from the first input clock signal when the second input clock signal is a constant signal at ground potential.

7. The method of claim 5 wherein the output clock signal is a single-ended clock signal generated when the input clock signal is determined to be a differential clock signal.

8. The method of claim 6 wherein the generated clock signal has the same frequency as either as the first input clock signal or the second input clock signal.

9. A device comprising:

a first terminal to receive a first clock input signal;

a second terminal to receive a second clock input signal; and

a detector coupled to the second terminal to receive the second clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second clock signal.

10. The device of claim 9 further comprising:

a first circuit coupled to the first terminal configured to generate a first single-ended clock signal of the same frequency as the first clock input signal;

a second circuit coupled to the first terminal and to the second terminal to generate a second single-ended clock signal of the same frequency as the first clock input signal; and

a selector configured to select the first single-ended clock signal or the second single-ended clock signal based upon the clock mode signal.

11. The device of claim 10 further comprising a clock generator coupled at least to the first terminal, configured to output a master clock signal.

12. The device of claim 11, further comprising a compensator configured to receive the signal from either the first circuit or the second circuit and to output a core clock signal aligned with the master clock signal.

13. The device of claim 12 wherein the compensator includes a phase-locked loop.

14. The device of claim 12 wherein the compensator includes delay cancellation as a function of the clock mode signal.

15. The device of claim 10 wherein the selector is a multiplexer.

16. A device comprising:

a switch including an input terminal and an output terminal;

a load coupled to the output terminal; and

a capacitor coupled to the output terminal;

wherein the input terminal receives a periodic clock signal; and

wherein the capacitor is so sized to filter out pulses caused by the oscillations of the clock signal applied to the input terminal of the switch.

17. The device of claim 16, further comprising an output buffer coupled to the output terminal.

18. The device of claim 16, wherein the switch comprises a field effect transistor and the input terminal comprises the gate of the field effect transistor.

19. The device of claim 16, wherein the switch transistor and the load are CMOS transistors.

20. A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; and

automatically generating a clock mode signal based on the determination.

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21. The method of claim 20 further comprising:

providing a first circuit for a single-ended clock signal, the output of the first circuit being a first output clock signal;

providing a second circuit for a differential clock signal, the output of the second circuit being a second output clock signal;

selecting either the output of the first circuit or the output of the second circuit as a function of the clock mode signal.

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22. A method comprising:

receiving a first periodic clock signal voltage at a first input;

receiving at a second input one of a second periodic clock signal voltage, a constant signal voltage above ground potential or a constant ground potential signal;

detecting whether the signal received at the second input is a constant ground potential signal; and

generating a clock mode signal indicative of the detection.

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23. The method of claim 22 further comprising generating a high voltage clock mode signal when the signal received at the second input is a constant ground potential signal.

24. A method comprising:

receiving a clock signal, wherein the clock signal is one of a single-ended clock signal or a differential clock signal; and

generating an output single-ended clock signal that follows the received clock signal.

25. The method of claim 24 further comprising aligning the output single-ended clock signal with the received clock signal.

26. A system comprising:

a clock generator, wherein the clock generator issues one of a single-ended clock signal or a differential clock signal; and

an electronic device including a first input terminal and a second input terminal, with the first input terminal coupled to the clock generator;

wherein the electronic device generates a single-ended clock signal of the same frequency as the clock signal issued by the clock generator.

27. The system of claim 26, wherein the electronic device issues a single-ended clock signal aligned with the clock signal issued by the clock generator.

28. The system of claim 26,

wherein the electronic device includes a first input terminal and a second input terminal, and

wherein the first input terminal is coupled to circuit ground when the clock generator issues a single-ended clock signal.

29. The system of claim 26,

wherein the electronic device includes a first input terminal and a second input terminal, and

wherein the first and second input terminals are coupled to the clock generator when the clock generator issues a differential clock signal.